LINEAR TECHNOLOGY

DESIGN NOTES

Hot Swapping the PCI Bus – Design Note 155

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The Peripheral Component Interconnect (PCI) bus has become widely used in high volume personal computers and single-board computer designs. With a 32-bit data path and a bandwidth of up to 133Mbps, PCI offers the throughput demanded by the latest I/O and storage peripherals. Unfortunately, the original PCI specification does not require the bus to be hot swappable, so the system power must be turned off when a peripheral is inserted into or removed from a PCI slot.

With the migration of the PCI bus into servers, industrial computers and computer telephony systems, the ability to plug a peripheral into a live PCI slot becomes mandatory. By using the LTC®1421 to control the power supplies and a QuickSwitch® bus switch to buffer the data bus, a peripheral can be inserted into a PCI slot without turning off the system power.

Inrush Current and Data Bus Problems

When the peripheral is inserted, the supply bypass capacitors on the peripheral can draw huge transient currents from the PCI power bus as they charge up. The transient currents can cause permanent damage to the connector

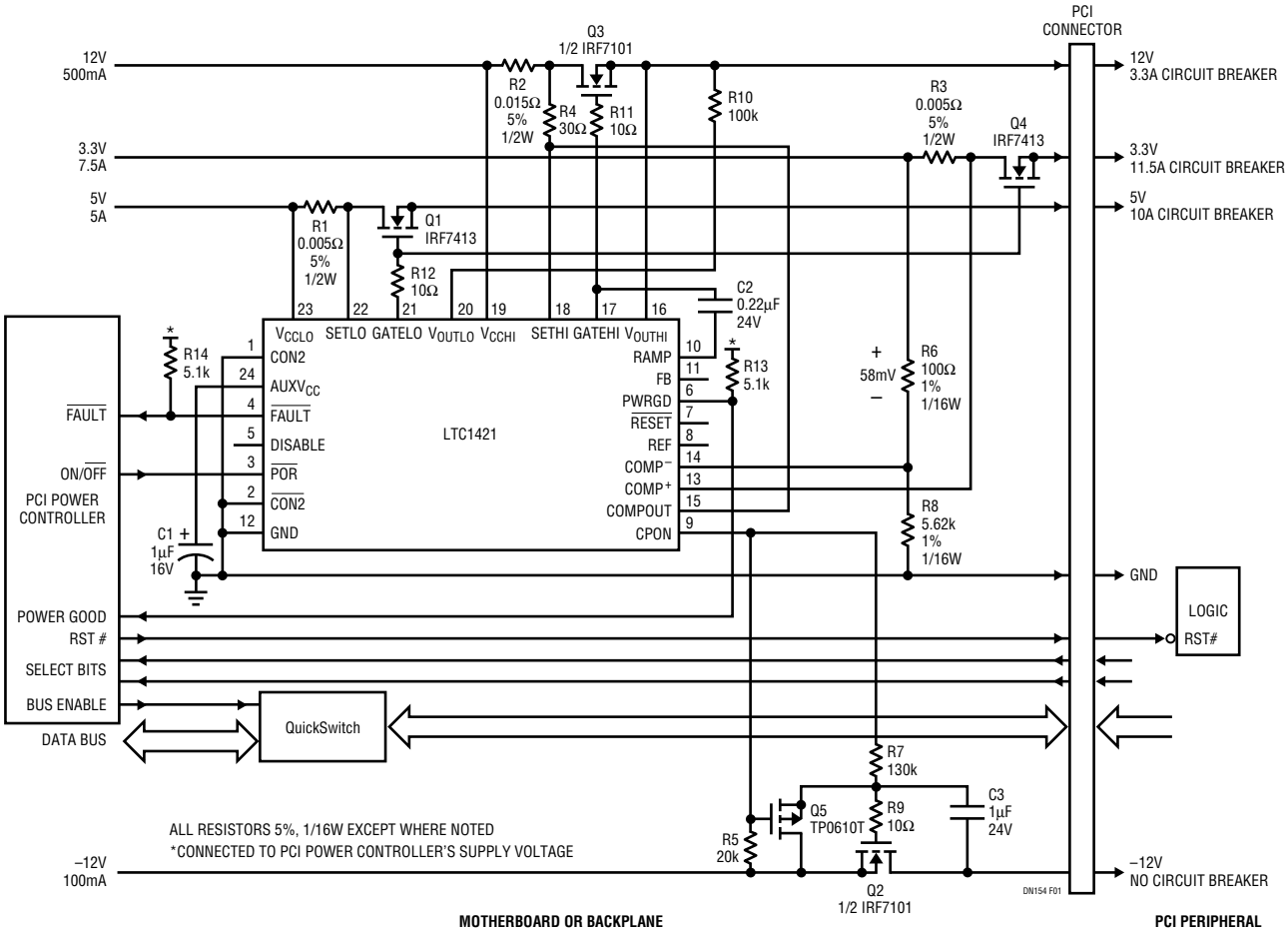

Figure 1. Hot Swappable PCI Slot

pins and board traces, while causing glitches on the system supply that force other peripherals in the system to reset.

The second problem involves the diodes to V_{CC} at the input or output of most logic families. With the peripheral initially unpowered, the V_{CC} input to the logic gate is at ground potential. When the data bus pins make contact, the bus lines are clamped to ground through the diodes to V_{CC} and the data is corrupted. With current flowing into the V_{CC} diode, the logic gate may latch up and destroy itself when power is applied.

Hot Swappable PCI Slot Using the LTC1421

The circuitry for a hot swappable PCI slot on a motherboard or backplane is shown in Figure 1.

The power supplies for each PCI slot are controlled by an LTC1421 and four external FETs, and the data bus is buffered by several QS3384 QuickSwitches or equivalent. A PCI power control ASIC, FPGA, microprocessor or the like, controls all of the slots within the system.

The 12V, 5V, 3.3V and –12V supplies are controlled by placing external N-channel pass transistors, Q1 to Q4, in the power path. By increasing the voltage on the gate of the pass transistors at a controlled rate, the transient surge current ($I = C \bullet dV/dt$) drawn from the PCI supplies can be limited to a safe value. The ramp rate for the positive supplies is set by $dV/dt = 20\mu A/C2$. The –12V supply ramp rate is set by R7 and C3, while resistor R5 and transistor Q5 help turn off transistor Q2 quickly. Resistors R9, R11 and R12 prevent potential high frequency FET oscillations. Resistors R13 and R14 pull up PWRGD and $\overline{FAULT}$ to the proper logic level.

Sense resistors R1, R2 and R3 provide current fault protection. When the voltage across R1 and R2 is greater than 50mV for more than 10µs, the LTC1421 circuit breaker is tripped. All of the FETs are immediately turned off and the $\overline{FAULT}$ pin is pulled low. The circuit breaker is reset by cycling the $\overline{POR}$ pin. The current fault protection for the 3.3V supply is provided by resistive divider R6 and R8 and the uncommitted comparator in the LTC1421. Because the current levels on the –12V supply are so low, overcurrent protection is not necessary.

The QuickSwitch bus switch contains a low resistance N-channel placed in series with the data bus. The switch is turned off when the board is inserted and then enabled after the power is stable. The switch inputs and outputs do not have a parasitic diode back to V_{CC} and have very low capacitance.

System Timing

The system timing is shown in Figure 2. The PCI power controller senses when a board has been inserted into the PCI via the power-select bits. Alternatively, the user can inform the controller that a board has been inserted via a front panel or keyboard. The PCI controller holds the RST# pin low and disables the QuickSwitch bus switches, then turns on the LTC1421 via the $\overline{POR}$ pin. The power supplies turn on at a controlled rate and when the 12V supply is within 10% of its final value, the PWRGD signal pulls high. The PCI power controller waits one reset time-out period and then pulls RST# high and enables the QuickSwitch devices.

When the board is turned off, RST# is pulled low, the QuickSwitch bus switches are disabled and the LTC1421 is turned off by pulling the $\overline{POR}$ pin low. After a 20ms delay, the external FETs are turned off and the supply voltages collapse.

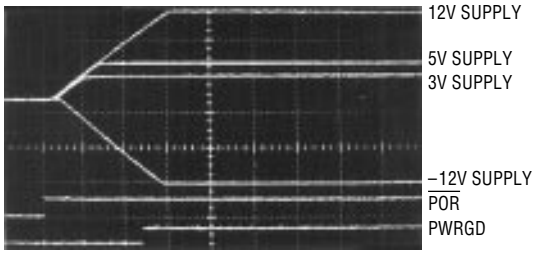

Figure 2a. Power Up

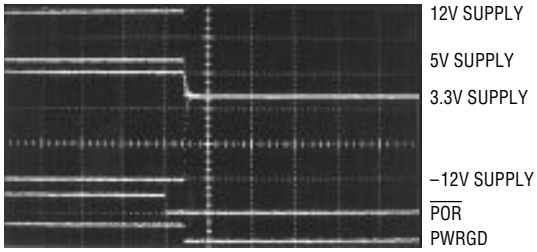

Figure 2b. Power Down

Conclusion

Using the LTC1421 and a QuickSwitch bus switch, a PCI slot can be made hot swappable so the system power can remain on when a peripheral is inserted or removed. Up to now, the design of Hot Swap™ circuitry has required the talents of an analog guru. With the LTC1421, safe hot swapping becomes as easy as hooking up an IC, a couple of power FETs and a handful of resistors and capacitors.

Hot Swap is a trademark of Linear Technology Corporation.

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